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BOOST-DERIVED HYBRID CONVERTER WITH SIMULTANEOUS DC AND AC OUTPUTS

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Abstract—This paper proposes a family of hybrid convertertopologies which can supply simultaneous dc and ac loads from a single dc input. These topologies are realized by replacing the controlled switch of single-switch boost converters with a voltage-source-inverter bridge network. The resulting hybrid con-verters require lesser number of switches to provide dc and ac outputs with an increased reliability, resulting from its inherent shoot-through protection in the inverter stage. Such multioutput converters with better power processing density and reliability can be well suited for systems with simultaneous dc and ac loads, e.g., nanogrids in residential applications. The proposed converter, studied in this paper, is called boost-derived hybrid converter (BDHC) as it is obtained from the conventional boost topology. The steady-state behavior of the BDHC has been studied in this paper, and it is compared with conventional designs. A suitable pulse width modulation (PWM) control strategy, based upon unipolar sine-PWM, is described. A DSP-based feedback controller is de-signed to regulate the dc as well as ac outputs. A 600-W laboratory prototype is used to validate the operation of the converter. The proposed converter is able to supply dc and ac loads at 100 V and 110 V (rms), respectively, from a 48-V dc input. The performance of the converter is demonstrated with inductive and nonlinear loads. The converter exhibits superior cross-regulation properties to dynamic load-change events. The proposed concept has been extended to quadratic boost converters to achieve higher gains.

Index Terms—Boost-derived hybrid converter (BDHC), dcnanogrid, pulsewidth-modulated inverters.

I. INTRODUCTION

Nano gridarchitectures are being increasingly incorpo-rated in modern smart residential electrical power systems [1]. These systems involve different load types—dc as well asac—efficiently interfaced with different kinds of energy sources (conventional or nonconventional) using power electronic con-verters [2]. Fig. 1 shows the schematic of a system, where a single dc source (v_{dcin}) (e.g., solar panel, battery, fuel cell, etc.) supplies both dc (v_{dcout}) and ac (v_{acout}) loads. The architecture of Fig. 1(a) uses separate power converters for each conversion type (dc–dc and dc–ac) while Fig. 1(b) utilizes a single powerconverter stage to perform both the conversions. The latter con-verter, referred to as a hybrid converter in this paper, has higher power processing density and improved reliability (resulting from the inherent shoot-through protection capability).These qualities make them suitable for use in compact systems with

both dc and ac loads. For example, an application of a hybrid converter can be to power an ac fan and a LED lamp both at the same time from a solitary dc input in a single stage

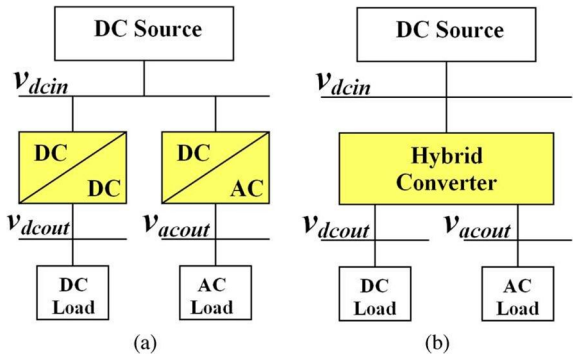


Fig. 1. Representative schematic of a nanogrid architecture with a single dc input and simultaneous dc and ac outputs. (a) Dedicated power converter-based architecture. (b) Hybrid converter-based architecture.

Smart residential systems are often connected to nonconven-tional energy sources to provide cleaner energy. Due to space constraints, these dedicated energy sources are highly localized and have low terminal voltage and power ratings (typically, on the order of a hundred watts). Conventional designs involve two separate converters, a dc–dc converter (e.g., boost) and a voltage source inverter (VSI), connected either in parallel [as shown in Fig. 2(a)] or in cascade [Fig. 2(b)], supplying dc and ac outputs at v_{dcout} and v_{acout}, respectively. Depending upon the requirements, topologies providing higher gains may be re-quired to achieve step-up operation [3]. This paper investigates the use of single boost-stage architecture to supply hybrid loads.

The operation of conventional VSIs in hybrid converters would involve the use of deadtime circuitry to prevent shoot-through. In addition, due to electromagnetic interference (EMI) or other spurious noise, misgating turn-on of the inverter leg switches may take place, resulting in damage to the switches. In residential applications, due to the compactness of the overall conversion system, the generation of spurious noise may be commonplace. Thus, the VSIs in such applications need to be highly reliable with appropriate measures against EMI-induced misgating.

The Z-source inverter (ZSI), proposed in [4], can mitigate the problem of shoot-through due to the EMI in a VSI. The use of a unique impedance network at the input of the ZSI allows a

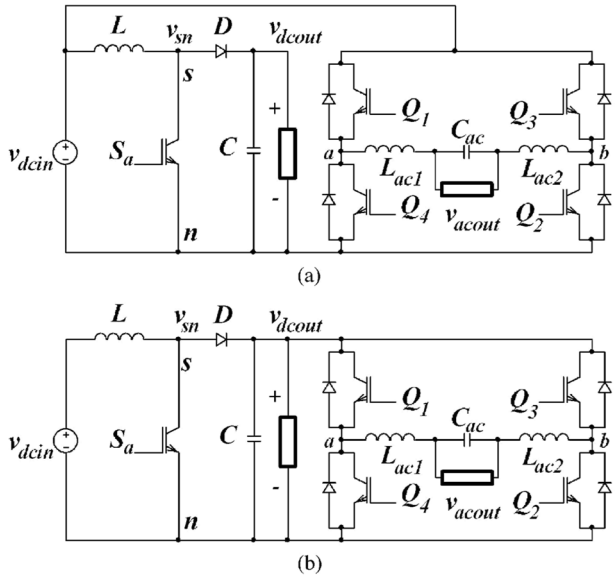


Fig. 2. Schematic of power converter topologies with simultaneous dc and ac loads. A conventional boost converter and a VSI have been used to implement the system. System (a) when both are connected in parallel and (b) when connected in cascade.

shoot-through state in which both the switches of an inverter leg can be turned on simultaneously. Extended boost ZSI has been proposed where a higher gain is achieved utilizing this Z-source topology [5]. However, ZSI cannot supply both dc and ac loads simultaneously. This is due to the fact that it has two capacitors which have to be matched with equal loads across them. Unmatched loads on the capacitors might lead to dynamic instability [6]. The switched boost inverter (SBI), proposed in [7], is a hy-brid converter topology, which can achieve similar advantages as a ZSI with lesser number of passive components and supply simultaneous dc and ac loads. This inverse Watkins–Johnson (IWJ) converter-derived topology [8] is a converter based

upon the first-order four-switch converter cell [9]. The proposed hybrid converter is derived from a two-switch converter cell-based step-up converter, such as the boost converter. There-fore, it involves lesser component count compared to the IWJ converter. The proposed converter is denoted as boost-derived hybrid converter (BDHC).

The objectives of this paper are the following: 1) to introduce a family of hybrid converter topologies capable of simultaneously supplying ac and dc loads; 2) to characterize the steady-state behavior of the BDHC topology; 3) to develop a PWM control scheme for the BDHC; 4) to compare the performance of the BDHC with conventional designs; 5) to validate the static and dynamic performance of the BDHC using an experimental prototype; and 6) to extend the proposed philosophy to higher order boost converters in order to achieve a higher conversion ratio.

This paper is organized as follows. The proposed circuit modification principle is described next in Section II, and its application to a boost converter is shown. The steady-state char-acterization of the converter is given in Section III. The PWM control strategy and the closed-loop implementation to regulate both ac and dc outputs are described in Section IV, followed by a comparative study of the BDHC in Section V. Section VI extends the circuit modification principle to higher order boost converters. The converter and its control strategy have been validated using an experimental prototype in Section VII.

II. BDHC

A. Proposed Circuit Modification

Boost converters comprise complementary switch pairs, one of which is the control switch (controls the duty cycle) and the other capable of being implemented using a diode. Hybrid con-verter topologies can be synthesized by replacing the controlled switch with an inverter bridge network, either a single-phase or three-phase one. The proposed circuit modification principle, applied to a boost converter, is illustrated in the next section. The resulting converter, called BDHC, is the prime focus area of this paper. Section VI extends this principle to higher order converters.

B. Derivation of BDHC Topology

The control switch S_a of a conventional boost converter [shown in Fig. 3(a)] has been replaced by the bidirectional single-phase bridge network switches (Q_1–Q_4) to obtain the BDHC topology [shown in Fig. 3(b)]. This proposed converter provides simultaneous ac output (v_{acout}) in addition to the dc output (v_{dcout}) provided by the boost converter.

For the BDHC, the hybrid (dc as well as ac) outputs have to be controlled using the same set of four controlled switches Q_1–Q_4. Thus, the challenges involved in the operation ofBDHC are the following: 1) defining the duty cycle (D_{st}) for boost operation and the modulation index (M_a) for inverter operation; 2) determination of voltage stresses and currents through different circuit components and their design; and 3) control and channelization of total input power to both ac and dc loads. In the subsequent sections, all the aforementioned challenges will be discussed.

III. OPERATION OF BDHC

The schematic of the BDHC with the reference current direc-tions has been shown in Fig. 3(b). In this paper, the continuous conduction mode of operation has been assumed (the boost inductor current (i_L) never goes to zero). In this paper, lower case letters represent instantaneous values, upper case letters represent dc or rms values, lower case letters with tilde represent the ac component, and lower case letters with (represent the peak value of the variable.

A. Operating Principle

Each of the four bidirectional switches (Q_1–Q_4) of BDHC comprises the combination of a switch S_i and an antiparallel diode D_i (i = 1 to 4). The boost operation of the proposed converter can be realized by turning on both switches of any particular leg (either S_1–S_4 or S_3–S_2) simultaneously. This is equivalent to shoot-through switching condition as far as VSI operation is concerned, and it is strictly forbidden in the case of a conventional VSI. However, for the proposed modification, this operation is equivalent to the switching "on" of the switch "S_a" of the conventional boost converter [see Fig. 3(a)].

The ac output of the BDHC is controlled using a modified version of unipolar sine-PWM switching scheme, described in Section IV. The BDHC, during inverter operation, has the same circuit states as a conventional VSI. The reason for this is as follows: For conventional VSIs (shown in Fig. 2), although the input to the bridge is a voltage stiff dc bus, the input dc voltage is required only during the power intervals, i.e., when there is a power transfer with the source. In the other intervals, the current freewheels among the inverter switches and these states do not require the input to be at a fixed dc value and hence can be zero. In the BDHC, the switch node voltage (v_{sn}) acts as the input to the inverter; it switches between the voltage levels—v_{dcout} and zero. The switching scheme should ensure that the interval for power transfer with the source occurs only when v_{sn} is positive, i.e., when v_{sn} is clamped to the dc output voltage v_{dcout}. Fig. 4 illustrates this concept.

The BDHC has three distinct switching intervals as described in the following.

1) *Interval I—Shoot-through interval*: The equivalent circuitschematic of the BDHC during the shoot-through interval is shown in Fig. 5(a). The shoot-through interval occurs when both the switches (either Q_1–Q_4 or Q_3–Q_2) of any particular leg are turned on at the same time. The duration of the shoot-through interval decides the boost converter duty cycle (D_{st}). The diode "D" is reverse biased during this period. The inverter output current circulates within the bridge network switches. Thus, BDHC allows ad-ditional switching states which are strictly forbidden in a VSI.
2) *Interval II—Power interval*: The power interval, shown inFig. 5(b), occurs when the inverter current enters or leaves the bridge network at the switch node "*s*." The diode "D" conducts during this period, and the voltage at the switch node (v_{sn}) is equal to the v_{dcout} (neglecting the diode voltage drop). In this interval, either Q_1–Q_2 or Q_3–Q_4 is turned on.
3) *Interval III—Zero interval*: The zero interval occurs whenthe inverter current circulates among the bridge network switches and is not sourced or sunk. The diode "D" con-ducts during this interval. Fig. 5(c) shows the equivalent circuit for this interval.

Fig. 4. Switch node voltage (v_{sn}), inductor current (i_L), inverter output voltage (v_{ab}), diode current (i_D), and inverter input current (i_{sn}) for a positive inverter output current. The reference directions for the voltages and currents have been shown in Fig. 3(b). The figure shows that the inductor current has a low-frequency component (at twice the power frequency) as described in Section III.

Table I shows the expressions for diode current (i_D), ca-pacitor current (i_C), inverter output voltage (v_{ab}), and boost switch node voltage (v_{sn}) for different operating modes. All these expressions have been defined in Fig. 3(b).

B. Steady-State Analysis

1) Gain Expression for DC and AC Outputs: Similar to conventional boost converters, the dc output of the BDHC can be regulated using the duty cycle, denoted by D_{st}, and is defined as the shoot-through time interval in a switching cycle, as shown in Fig. 4. For the purpose of analysis, we assume that the output dc capacitor voltage and the input inductor current have small ripple compared to their dc values. Hence, the expression for the voltage gain of the dc output is similar to that of a boost converter and can be derived as

$$\frac{V_{dco}}{V_{dcin}} = \frac{1}{1 - D_{st}}. \quad (1)$$

The modulation index, denoted by $M_a (0 \leq M_a \leq 1)$, regulates the ac output voltage of the BDHC, and its definition is similar

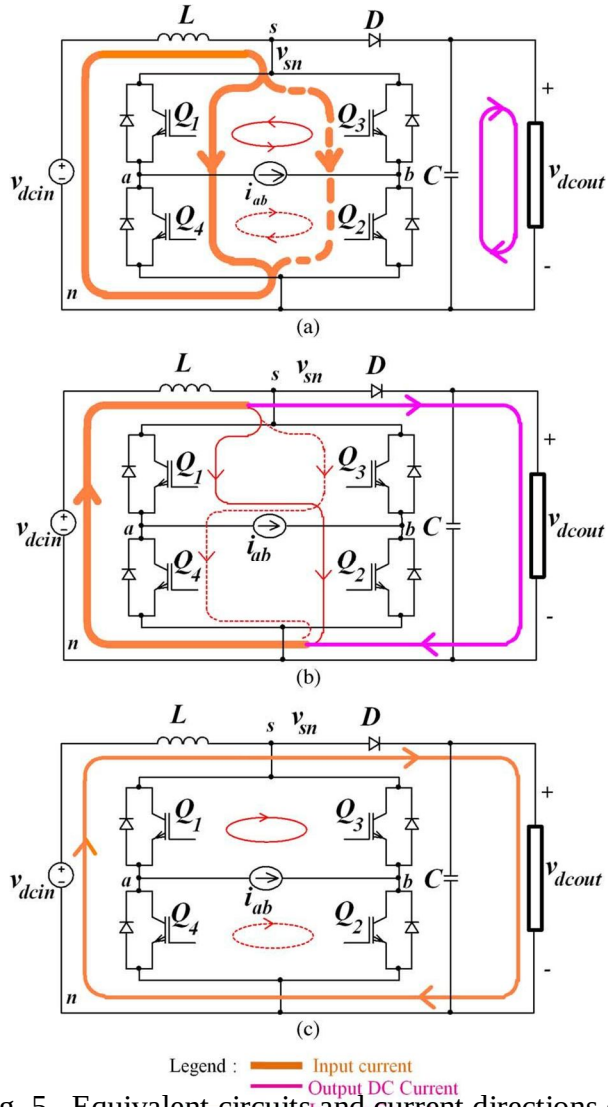


Fig. 5. Equivalent circuits and current directions of the BDHC during
(a) shoot-through interval, (b) power interval, and (c) zero intervals.

to that associated with conventional VSIs. The peak output ac voltage is related to the input as

$$\frac{\hat{v}_{acout}}{V_{dcin}} = \frac{M_a}{1 - D_{st}}. \quad (2)$$

The maximum dc output gain achieved using the BDHC is similar to that of boost converters and is around four to five [15].

The ac gain increases with the increase of modulation index (M_a) for any fixed value of duty cycle D_{st}. As the same set ofswitches controls both the dc and ac outputs, there is limitation to the maximum duty cycle or modulation index that can be achieved for this topology. The switching strategy must satisfy the following constraint:

$$M_a + D_{st} \leq 1. \quad (3)$$

Hence, the maximum value of ac gain is achieved at the equality condition of relation (3). At this condition, the peak value of the ac voltage is equal to the input voltage, and this is independent of the values of the duty cycle and modulation index. This can be obtained using (2) and (3). In order to achieve an ac voltage with voltage levels higher than the input voltage, either a step-up transformer needs to be interfaced to the BDHC or a higher order boost converter needs to be used, as will be explained in Section VI.

2) DC and AC Output Power Expressions: From (1) and (2),the expressions for output dc (P_{dc}) as well as ac power (P_{ac}) can be derived as follows:

$$P_{dc} = \frac{V_{dcin}^2}{R_{dc}*(1-D_{st})^2} \quad (4)$$

$$P_{ac} = \frac{0.5*V_{dcin}^2*M_a^2}{R_{ac}*(1-D_{st})^2}. \quad (5)$$

$R_{dc}$and $R_{ac}$are the dc and ac output resistances, respectively.Expressions (4) and (5) show that dc output power depends only on duty cycle (D_{st}), while ac output power depends upon both $D_{st}$and M_a.

3) Design of Passive Components: The ac output wave-forms of the BDHC are similar to those of a conventional VSI. Therefore, the filter design principles associated with the design of conventional VSIs can be used for L_{ac}($=L_{ac1}+L_{ac2}$) and C_{ac} [see Fig. 3(b)]. As far as the dc–dc converter filters are concerned, the selection of inductor (L) and capacitor (C) values depends mainly on the amount of allowable ripple in the inductor current and capacitor voltage. One of the

major differences between the BDHC and a conventional boost con-verter is that, in case of BDHC, since both dc and ac outputs are achieved, the inductor current (i_L) and the capacitor voltage (v_{dcout}) have both a high- and a low-frequency component (attwice the output ac power frequency), in addition to their dc values.

The ripple content due to the low-frequency component can be evaluated as follows. The instantaneous power input into the bridge network consists of a dc value (equal to P_{ac}) and sinusoidal component varying at twice the power frequency. In conventional VSIs, a dc-link capacitor is often used at the input, and this maintains the instantaneous power balance. This results in ripple content at the dc-link voltage at twice the power frequency. For the proposed converter, this instantaneous power balance is maintained by both the reactive elements (capacitor *C* and inductor *L*). Neglecting switching frequency components, the equations related to the instantaneous power balance can be written as follows.

For the BDHC, the inductor current is drawn from a dc source, and hence, the ripple content in the input current should be as low as possible. If the ripple in inductor current is fixed, the ripple in dc output can be calculated from (10).

4) Switch Stress and Current Expressions: The switches Q_1–$Q_4$and Q_3–$Q_2$are complementary in operation except dur-ing the shoot-through interval. The input to the inverter bridge equals to v_{dcout} (shown in Fig. 4) during both power and zero intervals. Thus, the maximum stress on each switch is equal to v_{dcout}, the dc output voltage, neglecting the voltage drop across the conducting diode D. The stress across the diode D is equal to v_{dcout} during the shoot-through interval. Thus, the selection of switch ratings is dependent upon the dc output voltage rather than the input voltage, contrary to the case for a conventional VSI.

As opposed to a conventional boost converter, the diode current (i_D) of BDHC is dependent upon the boost inductor current as well as the current drawn by the VSI bridge legs. This is due to the fact that, apart from the shoot-through interval, which is similar to the boost interval of a boost converter, there is an additional power interval. The current i_{sn} [shown in Fig. 3(b)] is equal to i_L during the shoot-through interval. During the power interval, i_{sn} equals the inverter output current i_{ab}. Since $i_{ab}$is time varying, the value of $i_{sn}$and, hence, diodecurrent i_D vary with time. This is shown in Fig. 4.

The expressions for the currents in different intervals are shown in Table I and in the Appendix (see Tables VI–VIII). The maximum current through the switches $\hat{i}_{sw}$ can be expressed as follows:

$$\hat{i}_{sw(i)} = \hat{i}_{L,max} + |\hat{i}_{ab}|, \quad (i = 1 \text{to} 4). \tag{11}$$

$|\hat{i}_{ab}|$ represents the maximum value of the inverter output cur-rent i_{ab}(t). Fig. 4 shows the nature of the switch node voltage (v_{sn}), inductor current (i_L), diode current (i_D), and inverterbridge input current (i_{sn}) for a positive value of ac output current (i_{ab}).

IV. CONTROL STRATEGY

A. Modified Unipolar PWM Strategy for BDHC

The fundamental principle behind the operation of BDHC is based upon the fact that the inverter bridge input must be connected to a positive voltage during the power interval only. This means that the inverter output has to be modulated when v_{sn} = 0 and boost operation occurs when v_{ab} = 0. The inverteroutput voltage assumes three different values, and hence, the PWM modulation strategy used is based upon unipolar sine-PWM scheme, which provides three voltage levels for output.

The PWM control scheme for the BDHC is based upon the switching scheme proposed in [10]. In this scheme, shown in Fig. 6(a), the shoot-through is realized by gating-on both the switches of a single leg at the same time. The switching strategy involves turning on only one leg at a time in order to achieve shoot-through. Another alternative is to turn on all the switches during shoot-through. This scheme has been proposed in [11] and [12], and the concept is illustrated using Fig. 6(b). As shown in the figure, turning on all the switches for shoot-

through involves more switching during each switching period with their associated losses. The reliability of the circuit also reduces since the time between two successive switching [switches S_1 and S_2 in Fig. 6(b)] is dependent on t_z, which

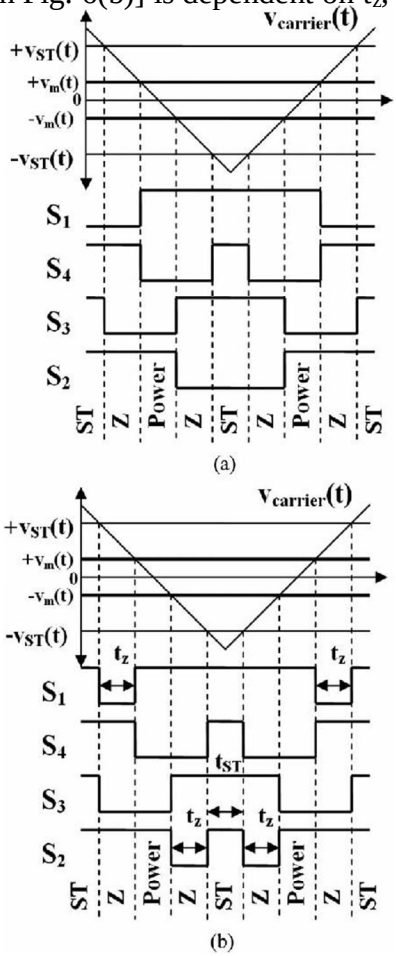
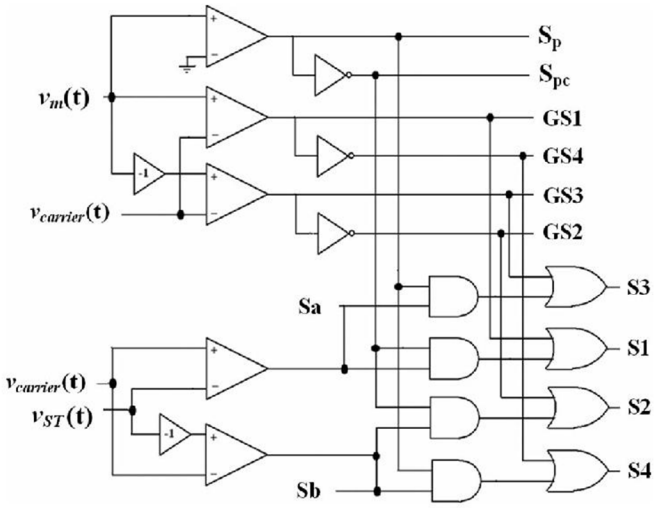
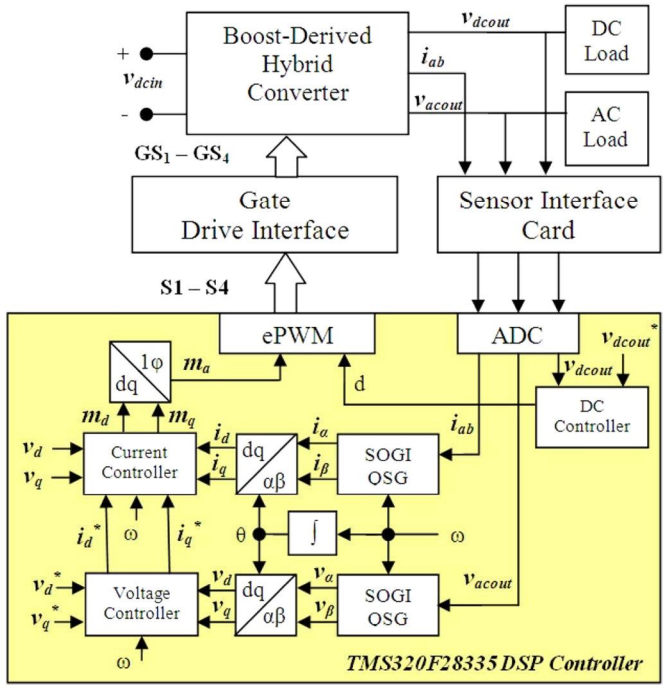


Fig. 7. Implementation of the PWM scheme shown in Fig. 6(a).





5) The current during the boost interval of the boost con-verter alternates between the two legs of the inverter. This enables the use of higher switching frequency for the boost converter, thus reducing the magnetic size and improving the dynamics of the system.
6) The converter can supply both ac and dc loads from a single dc input supply. The converter can also be adapted to generate ac outputs at frequencies other than line frequencies by a suitable choice of the reference carrier waveform.

The major limitation for the BDHC is that the degree of freedom is reduced when the relation (3) reaches equality condition. Another limitation for the converter is that, compared to the circuit of Fig. 2(b), the peak value of the ac output is less than the input voltage. However, for the ac output voltage realized using the configuration shown in Fig. 2(a), in practical situations, the maximum modulation index is around 0.85, which makes the maximum peak ac voltage to be 0.85 times the input. A similar peak ac voltage can be achieved by the BDHC using a lower modulation index by having a suitable value of the duty ratio.

VI. HIGHER ORDER BOOST-BASED HYBRID TOPOLOGIES

The maximum output-to-input gain achieved by the boost converter is limited to approximately four due to resistive losses [15]. Higher order boost converters with a single controllable switch have been described in [16]–[18], which achieve higher gains compared to a boost converter. Fig. 9 shows the schematic of the quadratic BDHC (QBDHC), which has been derived from the single-switch controlled quadratic boost converter. Thus, in general, the family of nth-order boost converters with single switch can be modified to form the corresponding family of hybrid boost converters.

VII. EXPERIMENTAL VERIFICATION

The behavior of hybrid converters, described in this paper, has been validated using a laboratory prototype. A 600-W IGBT-based laboratory prototype has been used to demonstrate the characteristics of the BDHC. For the purpose of designing the passive components, the ripple contents (both high- and low-frequency components) in the inductor current and the capacitor voltage have been taken to be 25% and 3%, respec-tively, at the rated power. Based on the equations described in Section III, the components for the BDHC have been de-signed. The controller of the prototype is implemented using the TMS320F28335 DSP kit. The SKYPER 32 Pro floating gate

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TABLE III
DESIGN EXAMPLE SPECIFICATIONS OF THE BDHC (OPEN-LOOP OPERATION)

Parameter		Attributes
Power Rating ($P_{dc} + P_{ac}$)		600 W
Input Voltage (V_{dcin})		48 V
Output Voltage	(V_{dcout})	100 V
	(V_{acout})	30 V rms
DC Load (R_{dc})		20 Ω
AC Load (R_{ac})		10 Ω
Switching Frequency		10 kHz

TABLE IV
PARAMETERS OF THE BDHC PROTOTYPE

Component	Attributes
Input Inductor (L)	5 mH
DC Capacitor (C)	1 mF
AC Filter Inductor ($L_{ac} = L_{ac1} + L_{ac2}$)	500 µH
AC Filter Capacitor (C_{ac})	10 µF

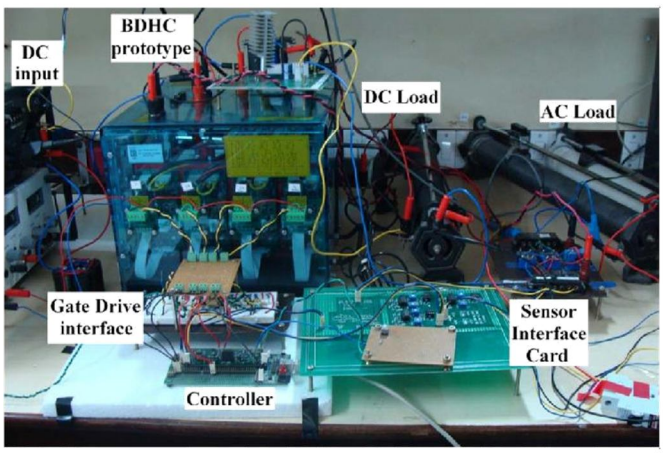


Fig. 10. Photograph of the IGBT-based laboratory prototype of the BDHC.

TABLE V
COMPONENT LIST

Component		Manufacturer
Switches	$Q_1 - Q_4$	SKM 100GB176d (Semikron)
	D	30EPH06 (Vishay)
Gate Driver		SKYPER 32 Pro (Semikron)
Controller		TMS320F28335 (TI)

drivers drive the IGBTs. A complete list of parameters and com-ponent values for the prototype is given in Tables III and IV. Fig. 10 shows the photograph of the experimental setup. Table V lists

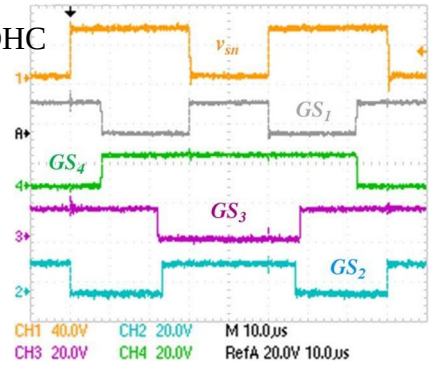
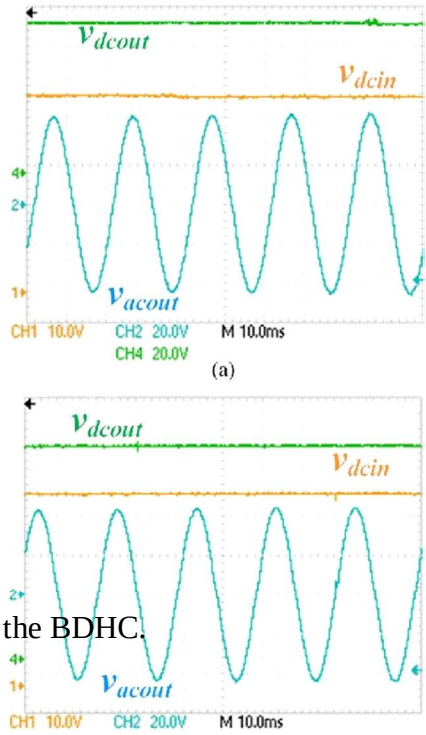


Fig. 11. Experimental validation of the proposed PWM control.



the components used for building the BDHC prototype.

A. Steady-State Behavior of BDHC

Fig. 11 shows the gate control signals for the BDHC switches and the resulting switch node voltage (v_{sn}) (referring to Figs. 3(b) and 8). The control schematic described in Section IV has been used for the generation of the gate signals. The waveforms validate that, whenever the switches S_1

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